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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/727,583	12/05/2003	Stephen K. Sunter	LVPAT065US	7341

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EXAMINER	
BRITT, CYNTHIA H	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 08/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/727,583	SUNTER ET AL.	
	Examiner	Art Unit	
	Cynthia Britt	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-19 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) 19 is/are allowed.

6)☒ Claim(s) 1-3, 7,8, 10,17 and 18 is/are rejected.

7)☒ Claim(s) 4-6,9,11-14 and 16 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 4/9/04, 12/5/03.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-19 are presented for examination.

Priority

Applicant's claim for domestic priority under 35 U.S.C. 119(e) is acknowledged.

Information Disclosure Statement

The information disclosure statements (IDS) submitted on December 5,2003 and on April 9, 2004 have been considered by the examiner. Forms 1449 have been signed and returned with this office action.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a)..

Claims 1-3, 7, 8, 10, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bridgewater, U.S. Patent No. 6,034,551 in view of Fan et al. PG Publication US 20040030968 A1

As per claims 1, 15, and 18 Bridgewater substantially teaches the claimed method and circuit using low-voltage differential signaling with a symmetrical driver and a dual receiver in order to provide for high-speed data communication and low-speed protocol communication. A high-speed receiver is used for data, and a low-speed receiver with a built-in offset is used for protocol information. (Figure 4, column 6 lines 19-67, column 7 line 59 through column 8 line 36) It is well known that if a high-speed serial communication link is implemented using metallic cable, a second fundamental problem of high-speed serial data links may also be encountered. The shield on a coaxial cable is typically tied to the signal ground plane of the printed circuit board from which the signal originated. If the shield is also tied to the signal ground plane of the receiver, ground loop problems, e.g. undesirable current flow and voltage drops, can

develop if the ground planes on the two circuit boards develop a potential difference between them. In order to eliminate this ground loop problem, AC-coupling may be used at the receiver end, using one capacitor to connect the coaxial cable center wire to a input conductor at the receiver and another capacitor to connect the shield of the coaxial cable to a ground conductor of the receiver. As is well known, these capacitors provide low impedances for high-frequency signals such as the high-speed data stream, but they also provide high impedances for the low frequency ground loop signals that might flow due to potential differences between the transmitter and receiver. However, in order for any AC-coupling to be used, the receiver system must guarantee a data stream that has an average density of logic 1's that is close to fifty percent, because a long-stream of logic 1's or logic 0's contains low-frequency signal components that will be filtered out and stored by the capacitors as DC levels, and the voltage on the output of the AC-coupled receiver will drift toward its bias point, which is usually the threshold of the decision circuit as well. As a result of this "DC wander" effect, the decision circuit will have difficulty differentiating between arriving logic 1's and arriving logic 0's, and the bit error rate on the serial communication link will increase if any noise is coupled into the link. Not explicitly disclosed is that the circuit can be used for testing.

However in an analogous art, Fan et al. teach that a test packet generator within a physical layer device, which generates test packets, to be communicated over a closed communication path established within the physical layer device. The test packets may include a pseudo-random bit sequence. A receiver within the physical layer device may receive at least a portion of the generated test packet. A test packet

checker within the physical layer device to compare at least a portion of the received test packets with at least a portion of the generated test packets in order to determine the bit error rate for the physical layer device. A window counter within the physical layer device to count at least a portion of a number of bits received within the generated test packets and a number of bits that are in error in at least a portion of the number of bits received. Accordingly, the bit error rate may be calculated based on a ratio of the number of counted bits in error to the number bits counted in the portion of the number of bits received (page 2 paragraphs 17-24 figure 6). Therefore it would have been obvious to a person having ordinary skill in the art at the time this invention was made to have combined the circuit of Bridgewater et al. with the testing circuit of Fan et al. This would have been obvious as suggested by Bridgewater et al. (column 4 lines 51-57) in order to have a receiver that allows high-speed data transmission to occur using a symmetrical driver, and for such a receiver to have excellent signal to noise margins for transmitting data at high-speeds and to conserve power.

As per claims 2 and 3, Bridgewater et al. teaches a high-speed receiver is used when transmitting data at high-speeds, and a lower performance, low-speed receiver is used for other SCSI phases. A built-in offset allows the low-speed receiver to operate correctly during bus arbitration. The built-in offset in the low-speed receiver takes the place of the termination bias voltage in a traditional SCSI bus and is implemented in a variety of ways. In a first example, an N-well generation circuit produces a bulk voltage for one transistor of the differential transistor pair that is different than a supply voltage supplied to the bulk of the other transistor. In a second example, each of the transistors

of the pair is implanted with a different dosage to change the threshold voltage for each. In a third example, resistors of different sizes are attached to the source of each transistor in the pair in order to produce a different voltage at each source. In a fourth example, two replica comparators are used to monitor an offset voltage of the differential receiver and to send control signals to an adjustable current source. The current source is adjusted by having an up-down counter switch on and off various legs of the current source. (Abstract, column 7 line 59 through column 8 line 36)

As per claims 7 and 8 the present application on page 2, (lines 8-19) paragraph 6 of the disclosure indicates the inherency of line impedance and the need for impedance termination.

As per claim 10, and 17, Fan et al. teach the calculation of bit error rates and the use of eye diagrams to determine proper operation. (pages 5-7 paragraphs 55, 63,and 79)

Allowable Subject Matter

Claims 4-6, 9, 11-14 and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 19 is allowable over the prior arts of record.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Publication No.US2002/0183003A1 Chang et al.

This publication teaches a wireless integrated circuit (IC) interconnection system, comprising: a wireless transmission medium, a transmitter which modulates a signal to be conveyed from a first IC location to a second IC location and provides said modulated signal at an output, a first capacitive coupler which capacitively couples said modulated signal from said transmitter output to said wireless transmission medium, a second capacitive coupler which capacitively couples said modulated signal from said wireless transmission medium to a receiver, said wireless transmission medium propagating said modulated signal from said first capacitive coupler to said second capacitive coupler, and a receiver which demodulates said modulated signal and provides said demodulated signal to said second IC location.

U.S. Patent No. 5,325,397 Scholz et al.

This patent teaches a method of assessing a link for a digital communication system and providing a value for a channel or link state parameter, particularly bit error rate, and apparatus for the same, in which an estimate of the probability density function for the channel or link is obtained by categorizing decision variables into threshold categories, and comparing the estimated probability density function with stored known probability density functions with each stored probability density function the value of

the channel parameter being monitored is stored. The value of the channel parameter being monitored is determined by selecting the value associated with the stored probability density function closest resembling the estimated probability density.

U.S. Patent No. 6,587,530 Conklin et al.

This patent teaches a signal integrity measurement method and apparatus which allows for signal characteristics to be measured by obtaining samples taken at the midpoint of the data stream. The invention provides a measurement device that is suitable for use in the field to provide a measurement of signal characteristics within transmitted data streams. The invention is particularly suitable for field measurement of signal characteristics of data streams or continuous in-line monitoring of signal characteristics within transmitted data streams. The signal characteristics include, but are not limited to eye opening jitter, noise, slope efficiency, average power and peak-to-peak amplitude.

U.S. Patent No. 5,606,317 Cloonan et al.

This patent teaches an apparatus for communicating data via a high speed serial data link. Serial data link has a parallel to serial converter, which accepts parallel data inputs having n bits, and converts the n bit groups of parallel data bits into a high speed serial data bit stream. This serial bit stream is connected to a serial data transmitter. Serial data transmitter receives the serial bit stream and drives the serial bit stream onto cable. The cable may be coaxial or twin axial, in which case serial data transmitter

would be a broad band power driver to overcome the capacitance of the cable without distorting the data wave form. Alternatively, cable may be optical, in which case serial data transmitter may be a laser or similar controlled light source. In either case, high-speed serial data is transmitted across cable at gigabit per second rates.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 703-308-2391. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Cynthia Britt
Examiner
Art Unit 2133

GUY J. LAMARRE
PRIMARY EXAMINER